

产品规格书

Specifcation of products

产品名称: 肖特基二极管

产品型号: MBRP400100CTT26

浙江世菱半导体有限公司
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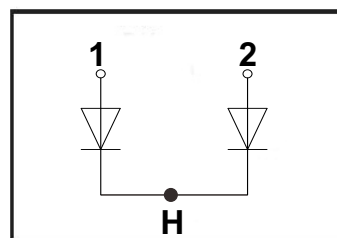
PRODUCT FEATURES

- Ultrafast Reverse Recovery Time
- Soft Reverse Recovery Characteristics
- Low Reverse Recovery Loss
- Low Forward Voltage
- High Surge Current Capability
- Low Inductance Package



APPLICATIONS

- Inversion Welder
- Uninterruptible Power Supply (UPS)
- Plating Power Supply
- Ultrasonic Cleaner and Welder
- Converter & Chopper
- Power Factor Correction (PFC) Circuit



ABSOLUTE MAXIMUM RATINGS

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Values	Unit
V_R	Maximum D.C. Reverse Voltage		100	V
V_{RRM}	Maximum Repetitive Reverse Voltage		100	V
$I_{F(AV)}$	Average Forward Current	$T_C=100^{\circ}\text{C}$, Per Diode	200	A
		$T_C=100^{\circ}\text{C}$, Per Moudle	400	A
$I_{F(RMS)}$	RMS Forward Current	$T_C=100^{\circ}\text{C}$, Per Diode	280	A
I_{FSM}	Non-Repetitive Surge Forward Current	1/2 Cycle , 60Hz, Sine	4000	A
I^2t	I^2t (For Fusing)	$T_J=45^{\circ}\text{C}$, $t=8.3\text{ms}$, 60Hz, Sine	11200	A^2s
P_D	Power Dissipation		525	W
T_J	Junction Temperature		-40 to +150	$^{\circ}\text{C}$
T_{STG}	Storage Temperature Range		-40 to +125	$^{\circ}\text{C}$
Torque	Module-to-Sink	Recommended (M6)	3~6	Nm
Torque	Module Electrodes	Recommended (M6)	3~5	Nm
$R_{\theta JC}$	Thermal Resistance	Junction-to-Case	0.20	$^{\circ}\text{C}/\text{W}$
Weight				g

ELECTRICAL CHARACTERISTICS

$T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{RM}	Reverse Leakage Current	$V_R=100\text{V}$	--	--	0.5	mA
		$V_R=100\text{V}, T_J=125^{\circ}\text{C}$	--	--	10	mA
V_F	Forward Voltage	$I_F=200\text{A}$	--	0.80	--	V
		$I_F=200\text{A}, T_J=125^{\circ}\text{C}$	--	0.70	--	V

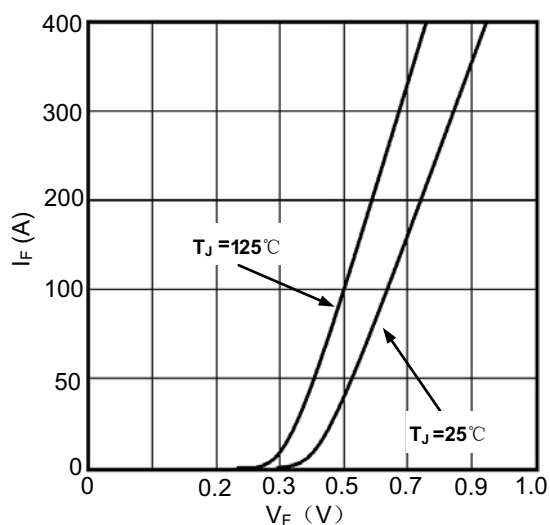


Figure1. Forward Voltage Drop vs Forward Current

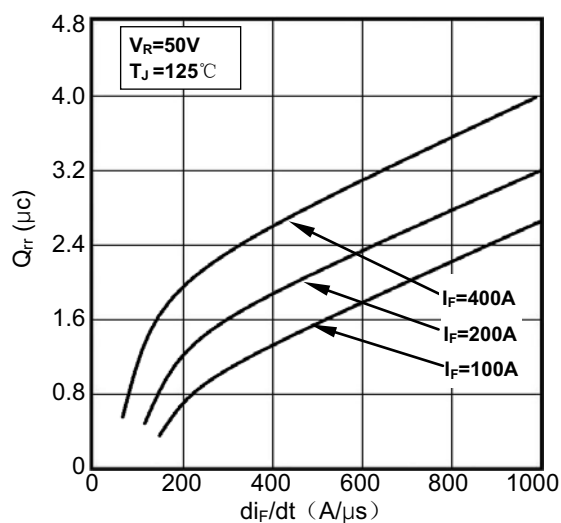


Figure2. Reverse Recovery Charge vs di_F/dt

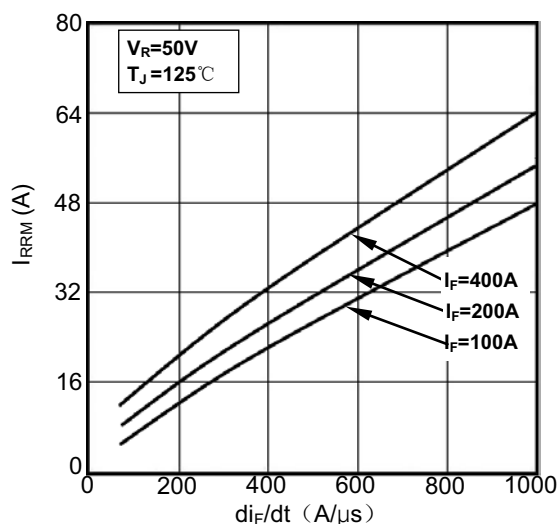


Figure3. Reverse Recovery Current vs di_F/dt

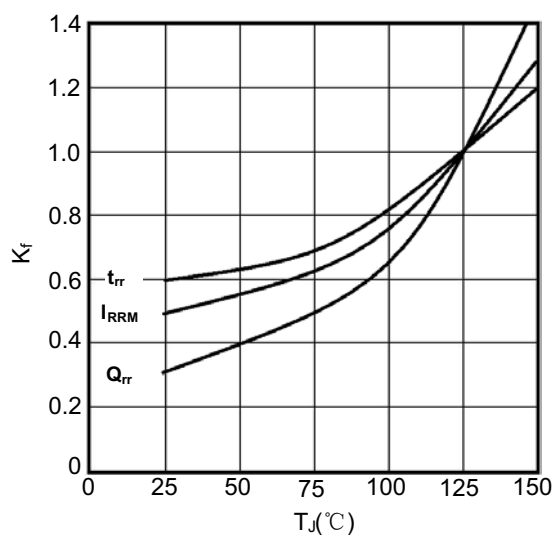


Figure4. Dynamic Parameters vs Junction Temperature

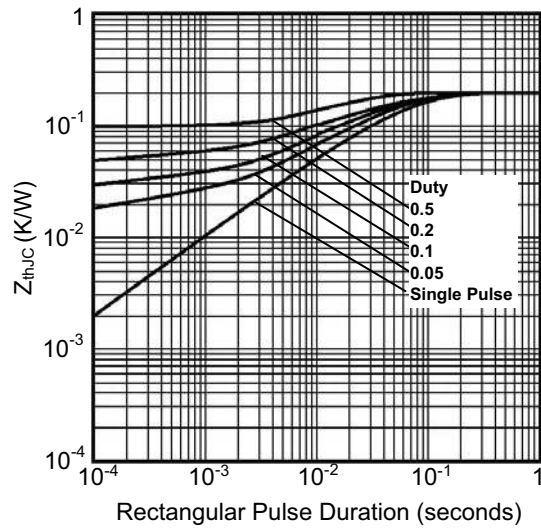


Figure6. Transient Thermal Impedance

Package Outline

